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Jameco Part Number 191863
(MC68HC11E1CP2)

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Motorola Semiconductor Engineering Bulletin

EB193

Replacing 68HC11A Series MCUs with 68HC11E Series MCUs

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Introduction

This information is presented to users of the MC68HC11A Family (A8/A1/A0) microcontrollers (MCUs) who are considering converting to MC68HC11E Family MCUs (E9/E1/E0).

The 68HC11E Family was designed to provide more ROM and RAM for 68HC11A users.

Both device families have the same pinouts in the 52-pin PLCC and 64-pin QFP (quad flat pack) packages.

The 68HC11E MCUs have several enhancements that require special design consideration.

Table 1 lists the major features of each device in the families.

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Table 1. 68HC11A and 68HC11E Features

Device	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	SCI	SPI	A/D	Input Only	Output Only	I/O
68HC11A8	8 K	256	512	Yes	Yes	Yes	Yes	11	12	15
68HC11A1	0	256	512	Yes	Yes	Yes	Yes	11	4	7
68HC11A0	0	256	0	Yes	Yes	Yes	Yes	11	4	7
68HC11E9	12 K	512	512	Yes	Yes	Yes	Yes	11	11	16
68HC11E1	0	512	512	Yes	Yes	Yes	Yes	11	3	8
68HC11E0	0	512	0	Yes	Yes	Yes	Yes	11	3	8

Basic Question and Answer

Can 68HC11Ax code run on 68HC11Ex without change?

No.

Pin Assignments

The A Family and E Family pinouts are identical for 52-pin PLCC and 64-pin QFP packages. On E Family pinouts, pin 31 of the 52-pin PLCC and pin 62 of the 64-pin QFP (quad flat pack) have additional functionality. This will be described in the Differences section under port A, bit 3.

Refer to the latest MC68HC11 E Family series technical databook while reviewing this information.

Converting from MC68HC11A to 68HC11E

Table 2 – showing differences, issues, and changes – describes the extent of analysis required for various MC68HC11A Family applications. In each case, the version of 68HC11A devices affected and the issues involved in converting to 68HC11E devices are identified.

Difference: ROM

The 68HC11E9 has 12 Kbytes of ROM at address locations $D000 through $FFFF, while the 68HC11A8 has eight Kbytes of ROM at address locations $E000 through $FFFF.

Case 1

Case: Single-chip mode, custom (masked) 68HC11A8 ROM devices

Issue: ROM code must be resubmitted.

Change required: Source code must be changed to address the EEPROM block protect and port A, bit 3 differences. Object code (S-records) must be resubmitted to Motorola.

Case 2

Case 2: Expanded mode, custom (masked) 68HC11A8 ROM devices

Issue: ROM code must be resubmitted.

Change required: Ensure that address space from $D000 through $DFFF is not used by external devices (memories or peripherals). Source code must be changed to address the EEPROM block protect and port A, bit 3 differences. Object code (S-records) must be re-submitted to Motorola.

Case 3

Case: Expanded mode, ROM-less 68HC11A1 or 68HC11A0 devices

Issue: Source code changes

Change required: Source code must be changed to address the EEPROM block protect and port A, bit 3 differences.

Table 2. Summary of Differences

Item	68HC11A	68HC11E	Issues
ROM	8 Kbytes located at $E000 to $FFFF	12 Kbytes located at $D000 to $FFFF	Source code changes; potential address conflicts in expanded mode
RAM	256 bytes located at $0000 to $00FF	512 bytes located at $0000 to $01FF	Potential address conflicts in expanded mode
EEPROM	512 bytes with no write protection	512 bytes with 4 selectable block protects	Block protection register (BPROT)
CONFIG register	Only programmable in special modes	Programmable in normal and special modes	CONFIG alteration; block protection
Port A, bit 3, PLCC pin 31, QFP pin 62	Output only pin shares output compare 5 with parallel output pin PA3	Bi-directional pin shares input capture 4 or output compare 5 with I/O pin PA3	Logic or circuitry connected to PA3
Bootstrap mode	Download terminates after all 256 RAM bytes are written	Download terminates after all 512 RAM bytes are written or after receiver detects 4 idle characters	Download duration
Registers	4 write-restricted registers	5 write-restricted registers; several registers have additional functionality	New registers; dual functionality; write restrictions; E clock disable

Difference: RAM

The 68HC11E Family has 512 bytes of RAM initially at address locations $0000 through $01FF, while the 68HC11A Family has 256 bytes of RAM at address locations $0000 through $00FF.

Case 1

Case: Single-chip mode, custom (masked) 68HC11A8 ROM devices

Issue: None

Change required: None. However, you may want to take advantage of the extra RAM space.

Case 2

Case: Expanded mode, custom (masked) 68HC11A8 ROM devices

Issue: Potential conflict with external memories

Change required: Ensure that address space from $0100 to $01FF is not used by external devices (memories or peripherals)

Case 3

Case: Expanded mode, ROM-less 68HC11A1 or 68HC11A0 devices

Issue: Potential conflict with external memories

Change required: Ensure that address space from $0100 to $01FF is not used by external devices (memories or peripherals)

Difference: EEPROM

Most devices in the 68HC11A and 68HC11E Families have on-board EEPROM.

The 68HC11E series has an additional protection mechanism to prevent inadvertent alteration of the CONFIG register and EEPROM contents due to program runaway. This feature is called block protect. The block protect register (BPROT) is used to disable the protection feature. This register must be accessed if EEPROM contents or the CONFIG register are allowed to be changed in the application.

Case 1

Case: Custom (masked) 68HC11A8 ROM devices, all operating modes

Issue: BPROT not implemented on 68HC11A8

Change required: Code in internal ROM must be changed to add the BPROT clearing instructions. User also may want to include the CONFIG verification routine suggested here.

Case 2

Case: ROM-less 68HC11A1 devices

Issue: BPROT not implemented on 68HC11A1

Change required: Code in external memory must be changed to add the BPROT clearing instructions.

Case 3

Case: ROM-less 68HC11A0 devices

Issue: BPROT not implemented on 68HC11A0

Change required: None, EEPROM not in memory map

Difference: CONFIG Register

The system configuration register (CONFIG) is implemented with EEPROM cells on most 68HC11 microcontrollers. The 68HC11A Family devices only allow changes of the CONFIG register in special modes (MODB pin held low during reset). The 68HC11E Family removes this restriction by allowing CONFIG reprogramming in normal operating modes. This enhancement was added to allow software to verify that the proper system configuration was attained and change it if necessary. See the section that follows on a CONFIG register verification procedure.

Case 1

Case: Custom (masked) 68HC11A8 ROM devices, all operating modes

Issue: CONFIG is modifiable only in special modes on 68HC11A8.

Change required: None, unless a CONFIG verification/modification routine is included in initialization code. If CONFIG can be modified by code, the CONFIG verification routine suggested here should be included and a new ROM code must be submitted.

Case 2

Case: ROM-less 68HC11A1 and 68HC11A0 devices

Issue: CONFIG is only modifiable in special modes on 68HC11A1 and 68HC11A0.

Change required: None, unless a CONFIG verification/modification routine is included in initialization code. If CONFIG can be modified by code, the CONFIG verification routine suggested here should be included.

Difference: Port A, Bit 3

The 68HC11A devices have three fixed input captures and five fixed output compares, and port A, bit 3 (PA3) is a dedicated output pin. On EX devices, this pin is bidirectional because it can be configured as a fourth input capture or a fifth output compare. The initial state of PA3 on 68HC11A devices after reset is active, driving low. The initial state of PA3 on 68HC11E devices after reset is input, high impedance.

Case 1

Case: All 68HC11A series devices

Issue: Logic or circuitry connected to PA3; pin 31 on PLCC; pin 62 on QFP (quad flat pack).

Changes required: A pulldown resistor is required on 68HC11E series MCUs to provide the same functionality as the 68HC11A during and immediately after reset. If the PA3 pin drives a high impedance input, a 4.7-K is adequate to initiate the low level. If the PA3 pin is driving an active circuit (transistor or other low impedance input), the bias circuit will have to be evaluated to determine proper functionality.

Additionally, software must be changed to configure the PA3 as an output driving a low level out of reset. If the PA3 pin is used as timer output OC5, the easiest procedure is to write $02 to the TCTL1 register which immediately configures the pin as OC5 driving low. (The BSET instruction with a mask of $02 can be used.) If the PA3 pin is used as an output pin (without the timer function), the procedure should include a write to the PORTA data register to drive bit 3 low and then a write to the PACTL register to set the DDRA3 bit.

NOTE: *If the PA3 pin is not used, it is still recommended that the pin be configured as an input and pulled up or down or configured as an output.*

Difference: Bootstrap Mode

The bootloader function on 68HC11A devices terminates a serial download to RAM after all 256 locations of RAM have been filled. Since 68HC11E devices have more RAM, the download procedure was changed to save download time. The 68HC11E bootloader terminates downloading after four idle characters have been received by the serial unit. Program control is then passed to the RAM.

Case: All 68HC11A series devices

Issue: Length of download

Change required: None. However, bootstrap downloads may execute faster if a program smaller than 256 bytes is downloaded. Also, a larger program may now be downloaded due to the additional RAM on the 68HC11E series.

Difference: Registers and Other I/O Control

Reads, writes, and compares of the following registers may have an effect on the system when switching between the 68HC11A and 68HC11E Families. The **bold text** in Table 3 represents the register or bit differences.

Table 3. Register Differences

Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	**PORTA**
$101E	Bit 15	14	13	12	11	10	9	Bit 8	**TI4O5 (high)**
$101F	Bit 7	6	5	4	3	2	1	Bit 0	**TI4O5 (low)**
$1021	**EDG4B**	**EDG4A**	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	**I4/O5I**	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	**I4/O5F**	IC1F	IC2F	IC3F	TFLG1
$1026	DDRA7	PAEN	PAMOD	PEDGE	**DDRA3**	**I4/O5**	RTR1	RTR0	PACTL
$1035	**0**	**0**	**0**	**PTCON**	**BPRT3**	**BPRT2**	**BPRT1**	**BPRT0**	**BPROT**
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO

MC68HC11A series MCUs have three input capture and five output compare channels on port A. The 68HC11A port A, bit 3 (PA3) pin is a dedicated output pin. On 68HC11E MCUs, this pin is bidirectional because it can be configured as a fourth input capture (IC4) or a fifth output compare. The PA3 pin state difference was covered earlier in this bulletin. Several other timer registers have been changed to allow the additional input capture function on 68HC11E devices.

PORTA

A read of this data register will return input data in bit positions 7, 2, 1, and 0 on 68HC11A devices. Bit 7 (PA7) can be configured as an output by software. A read of this register on 68HC11E devices will return input data in bit positions 7, 3, 2, 1, and 0. Bit 3 (PA3) can be configured as an output by software as stated in the port A, bit 3 section above.

TOC5 or TI4O5

The 16-bit register at $101E is the timer output compare 5 register on 68HC11A devices. On 68HC11E devices, this register is either timer input capture 4 register or output compare 5 register, depending on the function enabled by the I4/O5 bit in the PACTL register. The default function of this register is output compare 5.

TCTL2

Bits 7 and 6 in this register, which are not implemented on 68HC11A devices, control the input capture edge for IC4 on 68HC11E devices. IC4 functions only if the I4/O5 bit in the PACTL register is set.

TMSK1

Bit 3 is the output compare 5 interrupt enable on 68HC11A devices. On 68HC11E devices, bit 3 is the input capture 4 interrupt enable when the I4/O5 bit in the PACTL register is set. Bit 3 is the output compare 5 interrupt enable when the I4/O5 bit in the PACTL register is cleared.

TFLG1

Bit 3 is the output compare 5 flag on 68HC11A devices. On 68HC11E devices, bit 3 is either the input capture 4 flag or the output compare 5 flag, depending on the function enabled by the I4/O5 bit in the PACTL register.

PACTL — Bits 3 and 2 in this register, which are not implemented on 68HC11A devices, control the function of port A, pin 3 on 68HC11E devices. Bit 3 is the data direction bit (DDRA3), and bit 2 configures the pin either as IC4 or OC5 when used for timing functions.

BPROT — 68HC11E devices have this additional time- and write-restricted register which protects blocks of EEPROM and the CONFIG register from unintentional programming or erasure. Protection must be disabled by clearing bits during the first 64 clock cycles after reset in normal modes to enable intentional EEPROM changes. Protection for CONFIG and EEPROM blocks can be re-enabled later by setting the appropriate bits.

HPRIO — On 68HC11A devices, bit 4 is the internal read visibility bit, which is used in the special modes to affect visibility of internal reads on the expansion data bus. On 68HC11E devices, bit 4 is the internal read visibility/not E control bit. This control bit serves the same function during operation in expanded mode. In single-chip and bootstrap modes, IRVNE can be set to disable the E clock output to reduce system noise and power.

Special Section: CONFIG Register Verification and Reprogramming Routine

To guarantee proper operation of EEPROM-based M68HC11 devices, the CONFIG register must be programmed correctly. A CONFIG register verification and reprogramming routine should be included at the beginning of critical M68HC11 programs.

This code is an example of how to verify and, if necessary, reprogram the EEPROM CONFIG register to ensure proper operation. These same results can be accomplished with less generic, user-specified code.

```
* (C) MOTOROLA, INC., 1995 (created 05/01/95)
*
* FILENAME: config.asm
*
* DESCRIPTION: This code checks the CONFIG register on an EEPROM-based
* HC11 device and reprograms it with the proper value if necessary.
*

REGBASE   equ       $1000    ;beginning of HC11 registers

* Offsets from the beginning of the register block.

TOC4      equ       $1C
TCNT      equ       $0E
TFLG1     equ       $23
BPROT     equ       $35
OPTION    equ       $39
PPROG     equ       $3B
CONFIG    equ       $3F

* The following register bit constants are needed.

OC4F      equ       $10
PTCON     equ       $10
CME       equ       $08
BYTE      equ       $10
ERASE     equ       $04
EELAT     equ       $02
EEPGM     equ       $01
```

Fill in the blank that follows with the desired CONFIG register value. Also, choose the appropriate delay based on E frequency.

```
* Other user constants should follow, including:

MY_CONFIG equ       $__                 ;CONFIG should be __
DELAY     equ       $7530               ;$7530 = 30,000 counts at 3 MHz
                                        ;$4E20 = 20,000 counts at 2 MHz
                                        ;$2710 = 10,000 counts at 1 MHz

* Program begins here.
```

Fill in the program starting address in the following blank.

```
START     org       $____               ;program starts here

          lds       #$00FF              ;set a valid stack pointer
          ldx       #REGBASE            ;set beginning of register block
          ldaa      CONFIG,X            ;read CONFIG
          cmpa      #MY_CONFIG          ;check for valid CONFIG
          beq       NORMAL              ;if CONFIG is OK, go on as usual
```

At this point, 49 cycles remain for modifications to be made to the time protected registers (TMSK2, BPROT, OPTION, and INIT), if necessary, on all HC11 devices.

```
          bclr      BPROT,X,PTCON       ;clear CONFIG protect bit

* CONFIG erase sequence.

          ldaa      #BYTE + #ERASE + #EELAT
          staa      PPROG,X
```

The EEPROM erase sequence requires that some data be stored to the byte being erased. The actual data stored and instructions used are irrelevant; it is only necessary to complete a memory write cycle to the location in question.

```
          staa      CONFIG,X            ;store something to CONFIG

          ldaa      #BYTE + #ERASE + #EELAT + #EEPGM
          staa      PPROG,X
          jsr       EEDELAY             ;wait 10 ms
          clr       PPROG,X             ;finish erase sequence

* CONFIG program sequence.

          ldaa      #ERASE + #EELAT
          staa      PPROG,X
          ldaa      #MY_CONFIG          ;desired CONFIG value
          staa      CONFIG,X
          ldaa      #ERASE + #EELAT + #EEPGM
          staa      PPROG,X
          jsr       EEDELAY             ;wait 10 ms
          clr       PPROG,X             ;finish program sequence

* Now allow clock monitor to reset the HC11 and latch the new CONFIG
* register value.

          bset      OPTION,X,CME        ;enable clock monitor reset
          tpa                           ;get condition code register
          anda      #$7F                ;enable STOP mode
          tap
          nop
          stop                          ;enter STOP mode and allow reset

* User program resumes normally here.

NORMAL    etc.

* This EEPROM delay subroutine may be used for any EEPROM programming
* or erase operations.

EEDELAY   ldd       TCNT,X              ;get current time
```

The #DELAY term used for program and erase operations is calculated as follows:

DELAY = ECLK 100

Typical decimal values for DELAY are 30000 at 3 MHz, 20000 at 2 MHz, and 10000 at 1ÊMHz. Note that these values apply when the timer prescale is divide-by-1.

```
          addd      #DELAY              ;add delay
          std       TOC4,X              ;allow match at end of delay
          ldaa      #OC4F               ;clear last OC4 match
          staa      TFLG1,X

* Wait for OC4 match (end of 10 ms delay) to occur.

DELAYLOOP brclr     TFLG1,X,OC4F,DELAYLOOP

          rts                           ;end of delay loop

*
```

Special Section: Using the HC11 A-Series PA3 Pin Functionality on the HC11 E-Series

Because of the specific differences stated earlier in this engineering bulletin, there must be small code changes to use the PA3 pin functionality when converting from the HC11 A-series to the HC11 E-series.

State of the PA3 Pin (Pin 31) in PORTA

This code is an example of how to change the HC11 E-series PA3 pin from a high impedance input to a logic 0 (output) as it is on the HC11 A-series.

```
*******************************************************************************
* Software that configures HC11 E-series PA3 pin as an output similar to the HC11*
* A-series. Instruction lines in BOLD denote a instruction changes that are       *
* different when using the E-series.
*******************************************************************************
* REGISTER CONSTANTS
REGBASE       EQU     $1000               ; start of register block
PACTL         EQU     $26
* BIT CONSTANTS
DDRA3         EQU     $08                 ; DDRA3 bit in PACTL register
                                          ; configures the PORTA pin 3
```

```
* START OF PROGRAM *
       .
       .
       .
       LDX     #REGBASE                    ; increment from beginning of register
                                           ; block
       BSET    PACTL,X,DDRA3               ; set ddra3 bit to configure PORTA
                                           ;  pin 3 as an output
       etc...
```

Using the Output Compare 5 on the HC11 E-Series

This code is an example of how to use the output compare 5 on the HC11 E-series. The output compare is used here as a simple 10 ms delay subroutine.

```
*******************************************************************************
* Example routine to use the different approach of the OC5 on the HC11 E-series which*
* is different from the HC11 A-series. The OC5 is used in a simple 10 ms delay in*
* this example. Instruction lines in BOLD denote a difference in the commands of the*
* HC11 A-series.
*******************************************************************************
* REGISTER CONSTANTS
REGBASE        EQU     $1000               ; start of register block
TCTL1          EQU     $20
TFLG1          EQU     $23
PACTL          EQU     $26
TCNT           EQU     $0E
TI4O5          EQU     $1E                 ; HC11 A-series devices contain the TOC5
                                           ; register at address $101E
* BIT CONTANTS
DELAY          EQU     $7530               ; 10 ms:
                                           ; $7530 = 30,000 counts @ 3 MHz
                                           ; $4E20 = 20,000 counts @ 2 MHz
                                           ; $2710 = 10,000 counts @ 1 MHz
DDRA3          EQU     $08                 ; DDRA3 bit in PACTL register
                                           ; configures the PORTA pin 3
I4O5           EQU     $04                 ; I4/O5 bit in PACTL register
                                           ; configures TI4/O5 register to
                                           ; either OC5 or IC4
I4O5F          EQU     $08                 ; I4/O5f bit is set when either an OC5 or
                                           ; IC4 has occurred depending on the state
                                           ; of the I4/O5 bit in the PACTL register
```

```
**  BEGINNING OF POSSIBLE SUBROUTINE FOR A 10-ms DELAY USING THE OC5  **

DLY10          LDX     #REGBASE              ; increment from beginning of register
block
       BSET    PACTL,X,DDRA3                 ; set ddra3 bit to configure PORTA
                                             ; pin 3 as an output
       BCLR    PACTL,X,I4O5                  ; clear bit to configure register
                                             ; as an output compare
       LDD     TCNT,X
       ADDD    #DELAY                        ; add 10 ms delay to value in counter
       STD     TI4O5,X
       BSET    TFLG1,X,I4O5F                 ; clear I4/O5F flag
LOOP   BRCLR   TFLG1,X,I4O5F,LOOP            ; wait for I4/O5f bit to be set
       RTS                                   ; return to program
```

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